WHAT IS CLAIMED IS:

1. A system for managing volatile storage of information for operating a device having extended periods of inactivity between periods of activity comprising:

volatile memory connected to receive said information from a source and enabled to retain said information during power-on conditions;

processing circuitry coupled to said volatile memory to process said information during said periods of activity; and

a volatile memory checker enabled to execute between said periods of activity, said volatile memory checker including test code configured to detect errors within said information retained in said volatile memory.

2. The system of claim 1 wherein said volatile memory, said processing circuitry and said volatile memory checker are integrated into a single integrated circuit chip, said test code being configured to detect soft errors.

3. The system of claim 2 wherein said volatile memory is one or both of dynamic random access memory (DRAM) and static random access memory (SRAM) embedded within said integrated circuit chip, said processing circuitry including a processing unit.

4. The system of claim 1 wherein said volatile memory checker includes a timing module enabled to trigger execution of said test code in response to detection of a passage of a preselected time period and simultaneous detection that said device is in a period of inactivity.

5. The system of claim 1 further comprising a recovery module responsive to said volatile memory checker to selectively trigger information replacement for said volatile memory upon detecting said errors, said information being executable code for operating said device.

6. The system of claim 5 wherein said recovery module is configured to selectively reinitialize said device to initiate a transfer of said executable code from said source to said volatile memory.

7. The system of claim 5 wherein said recovery module is configured to selectively reset said device in response to a system-wide error in execution of said executable code.

8. The system of claim 5 wherein said volatile memory checker is configured to perform a cyclic redundancy check (CRC) or checksum of executable code memory space of said volatile memory.

9. The system of claim 1 wherein said volatile memory, said processing circuitry and said volatile memory checker are integrated into an application specific integrated circuit (ASIC) of a printer controller.

10. The system of claim 1 wherein said volatile memory and said processing circuitry are housed within separate integrated circuit chips.

11. A method of assessing integrity of executable code comprising the steps of:

transferring said executable code into volatile memory of a device that is activated upon execution of said executable code, said device being in an inactive state between executions of said executable code;

performing time-based volatile memory checking routines in response to detecting that said device is in said inactive state and a preselected time period has elapsed, including checking code space of said volatile memory to detect errors within said executable code; and

initiating a selected response upon detecting fatal code error during performing said checking routines.

12. The method of claim 11 wherein said step of performing said routines includes calculating a cyclic redundancy check (CRC) or checksum for executable code space of said volatile memory.

13. The method of claim 11 wherein said step of initiating said selected response includes triggering a reinitialization that repeats said step of transferring said executable code into said volatile memory.

14. The method of claim 13 wherein said step of initiating further includes resetting said device in response to a code error that results in said checking routines being terminated.

15. The method of claim 11 wherein said step of transferring includes loading said executable code into random access memory embedded in an integrated circuit having a central processor.

16. The method of claim 15 wherein said step of performing said checking routines includes scheduling said checking routines to occur on a periodic basis.

17. An integrated circuit comprising:

a processor;

embedded volatile memory having an input to receive executable code that includes instructions specific to operations of said processor;

an integrated self-tester having stored test code specific to detecting code error in said executable code during storage in said volatile memory, said self-tester being responsive to a time-based test initialization signal for triggering periodic testing; and

a recovery module responsive to said self-tester to induce an operational sequence that transfers fresh executable code to said input of said volatile memory when said self-tester detects a specific code error condition.

18. The integrated circuit of claim 17 wherein said volatile memory is one or both of dynamic random access memory (DRAM) and static random access memory (SRAM), said specific code error condition including alpha particle-induced error detections that are pre-identified as being fault conditions.

19. The integrated circuit of claim 17 wherein said self-tester includes embedded non-volatile memory for storing said test code.

20. The integrated circuit of claim 17 wherein said processor and said executable code are specific to operating within a printer controller.

21. The integrated circuit of claim 17 wherein said recovery module includes code for inducing reinitialization in which said volatile memory is reloaded with said executable code from a source of said executable code.

22. A system for managing information storage comprising the steps of:

storing said information within memory that is susceptible to occurrences of soft errors, said memory being within a device that is characterized by extended periods of inactivity between periods of activity;

processing circuitry coupled to said memory to process said information during said periods of activity; and

an automated memory checker enabled to execute between said periods of activity, said automated memory checker being configured to execute test code on a timed basis to detect said soft errors within said information stored in said memory.

23. The system of claim 22 wherein storing said information in memory includes magnetically recording said information on a medium susceptible to said occurrences of soft errors.

24. The system of claim 22 wherein storing said information includes embedding said information within non-volatile memory housed within an integrated circuit chip, wherein said non-volatile memory is susceptible to said occurrences of soft errors.